CRD42L52

Reference Design and Peripheral Driver Board for CS42L52

Reference Design Board (CRD42L52) Features

- Ultra-Small Layout
- Stake Header for External System Connections
- 1/8” Stereo Input Allows up to 2 Vrms Signals
- 1/8” Stereo Headphone Output Jack
- Built-in Switch Control for CS42L52 SPKR/HP Pin
- Stereo Full Bridge Speaker Output Terminal
- Complies with FCC class B and CISPR 22 Standards for Radiated Emissions

Peripheral Driver Board (CDB42LDB1) Features

- Multiple Power Supply Options
  - Three AAA Battery Source
  - External Power Supply Header
- S/PDIF I/O (CS8416 Receiver)
  - Optical and RCA Input Jacks
- S/PDIF I/O (CS8406 Transmitter)
  - Optical and RCA Output Jacks
- FlexGUI S/W Control - Windows® Compatible
  - Pre-Defined & User Configurable Scripts

Description

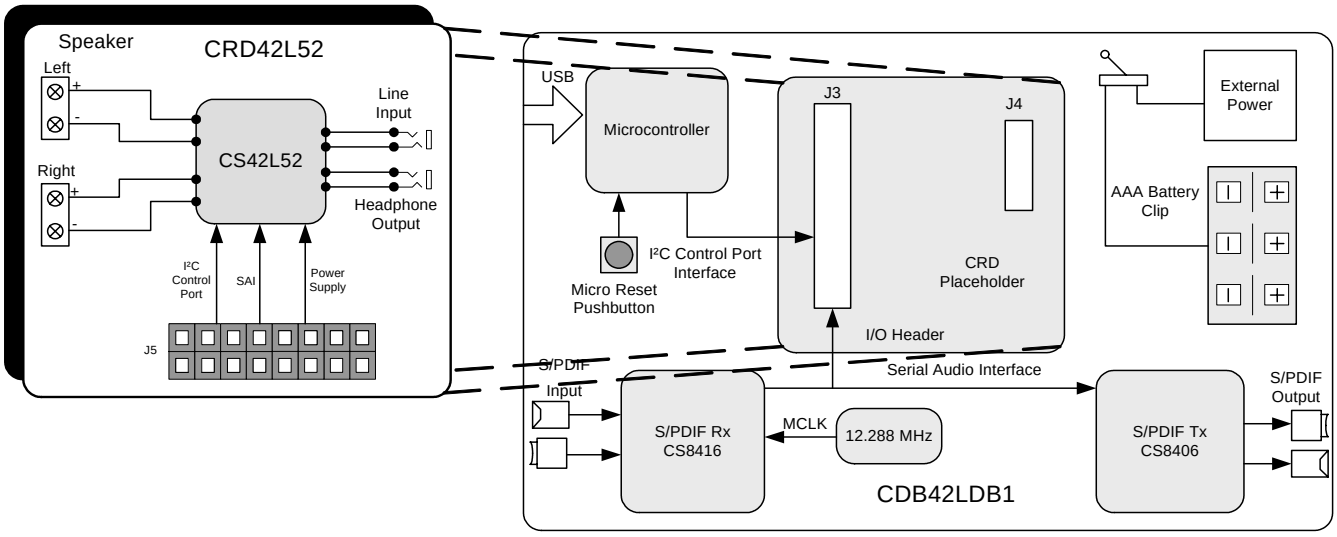
In addition to providing a reference for an ultra small layout design, the purpose of the CRD42L52 is to allow a quick and easy evaluation of the CS42L52 low power stereo CODEC.

Two 1/8” stereo jacks on the CRD42L52 provide an interface for analog line-level input and headphone-level output connections to the CS42L52. Stereo differential PWM speaker outputs from the CS42L52 can be monitored on a pair of screw terminals on the CRD42L52. The control port and serial audio interfaces are accessible via the I/O stake header used to attach the CRD42L52 to the CDB42LDB1.

The CDB42LDB1 is a peripheral driver board that provides clock/data, control logic and power supply to the CRD42L52. Digital data is transmitted and received via S/PDIF optical and RCA connectors. The CRD42L52 can be programmed by using the Windows Compatible FlexGUI software provided. Power is derived either from three AAA batteries or from an external supply on the CDB42LDB1 driver board and is routed to the CRD42L52 via the I/O stake header.

ORDERING INFORMATION

CRD42L52	Reference Design
CDB42LDB1	Driver Board



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1. SYSTEM OVERVIEW

The CRD42L52 provides a quick and general overview of the features in the CS42L52 CODEC in addition to providing a reference for an ultra-small layout design.

Line, headphone and PWM terminals are accommodated on the board for part evaluation and measurement purposes. The control port and serial audio interfaces are accessible via the I/O stake header used to attach the CRD42L52 to the CDB42LDB1. The driver board consists of a S/PDIF receiver, a S/PDIF transmitter and a USB microcontroller and is used to provide data to the CRD42L52. Therefore, in order to operate the CRD42L52 and use the Cirrus FlexGUI software to configure it, it must be connected to the CDB42LDB1 reference design board. This section serves to give a general overview of the hardware components used on the CRD42L52 reference design board and the CDB42LDB1 peripheral driver board.

1.1 Power (U2)

Power can be supplied to the boards by using one of the two power supply options on the CDB42LDB1 driver board. Power is supplied to the driver board either from 3 AAA +1.5 V batteries (placed on the battery clips behind the driver board) or from an external power supply (J1). The desired power supply must be selected using the appropriate setting on switch S1. The power supply on the driver board is regulated down to 3.3 V and 1.8 V as shown in the schematic (Figure 23 on page 22) to provide power to the various components on the driver board. The I/O header (J3) also contains power supply lines to route a 1.8 V supply line to power the analog and digital cores of the CS42L52 on the CRD42L52 board.

1.2 Microcontroller (U3)

The USB microcontroller on the CDB42LDB1 driver board drives the I²C® control port interface lines to the CRD42L52 via an I/O stake header and is used to configure the CS42L52. The microcontroller is also used to enable the CDB42LDB1 to drive the digital audio data and clock lines.

On-board functionality can be controlled by selecting appropriate configuration settings in the provided Windows-compatible FlexGUI software. For a detailed description of the Cirrus FlexGUI software, refer to Section 4. "Software Mode Control".

1.3 CS8416 Digital Audio Receiver (U7)

The CS8416 is a S/PDIF receiver that converts the S/PDIF data stream received by the board via either the optical or RCA phono connector into PCM data. This PCM data is routed to the I/O stake header which routes it to the CS42L52 on the CRD42L52 board.

The CS8416 is configured to operate in hardware master mode and provides the system master clock when a S/PDIF input source is connected to the board. Should the S/PDIF source become unavailable, causing a Receiver Error, the system clock is automatically switched to the one provided by the on-board oscillator for uninterrupted operation of other on-board components receiving the master clock.

A complete description of the CS8416 receiver and a discussion on the digital audio interface are included in the CS8416 data sheet.

1.4 CS8406 Digital Audio Transmitter (U8)

The CS8406 is a S/PDIF transmitter that converts the PCM data it receives from the I/O stake header into a S/PDIF data stream. The S/PDIF data can be monitored either via the optical (J7) or RCA phono connector (J9) on the CDB42LDB1 driver board. The CS8406 is configured to operate in hardware slave mode. It receives its clocks from the CS8416. In the case of a receiver error, the clock source for the CS8406 is automatically switched to the on-board oscillator for uninterrupted operation of the CS8406.

A complete description of the CS8406 transmitter and a discussion on the digital audio interface are included in the CS8406 data sheet.

1.5 Oscillator (Y1)

The on-board oscillator provides the system master clock when the digital audio receiver is powered down or when a receiver error occurs in the CS8416. Internal circuitry in the CS8416 automatically sets the oscillator clock as the new system clock whenever a receiver error is detected. This feature allows users to operate the boards without having a S/PDIF input fed to the board at all times.

1.6 CS42L52 Audio CODEC (U1)

A complete description of the CS42L52 (Figure 21 on page 20) is included in the CS42L52 product data sheet. The CS42L52 is configured using the Windows-compatible Cirrus FlexGUI software provided. The I²C control port interface on the CS42L52 can be used for register manipulation and is controlled by the microcontroller on the CDB42LDB1 driver board.

For full details on software functionality, refer to Section 4. "Software Mode Control".

1.7 Analog Input

A 1/8" stereo jack can be used to supply stereo line-level analog inputs to the CS42L52 up to a full-scale value of 2 Vrms. An AC-coupled passive filter and a voltage divider scale down the signal before sending it to the CS42L52 to prevent the signal from clipping.

The CRD42L52 is routed to only allow analog inputs on input channel 1 of the CS42L52. Analog Input Channels 2, 3 and 4 and Microphone Input Channels 1 and 2 are not connected.

1.8 Analog Outputs

The analog output from the CS42L52's ground-centered headphone amplifier can be monitored on the 1/8" stereo jack on the CRD42L52. Alternatively, one can also monitor the differential stereo PWM speaker output on the CS42L52 by using the differential speaker terminals J3 and J4.

1.9 Layout

The CS42L52 requires only a minimal set of components to achieve specified performance results. Its integrated ground-centered amplifier eliminates the need for bulky DC-blocking capacitors and only requires two tiny ceramic capacitors for the charge pump. Additional components include load-stabilization circuitry and power supply decoupling. See the CS42L52 data sheet for further details.

Figure 20 on page 19 provides an overview of the connections to the CS42L52. Figure 24 on page 23 and Figure 25 on page 23 show the component placement. Figure 26 on page 23 shows the top layout; Figure 27 on page 23 and Figure 28 on page 23 show the inner layers, and Figure 29 on page 23 shows the bottom layout. The decoupling capacitors are located as close to the CS42L52 as possible. Extensive use of ground plane fill in the reference design yields large reductions in radiated noise.

2. QUICK-START GUIDE

The following figure is supplied for user convenience as a simplified quick-start guide. Refer to Section 1 on page 4 and Section 3 on page 7 for details on how the various components on the board interface with each other in the different configuration modes. Refer to Section 4 on page 9 for descriptions on control settings in the Cirrus FlexGUI software.

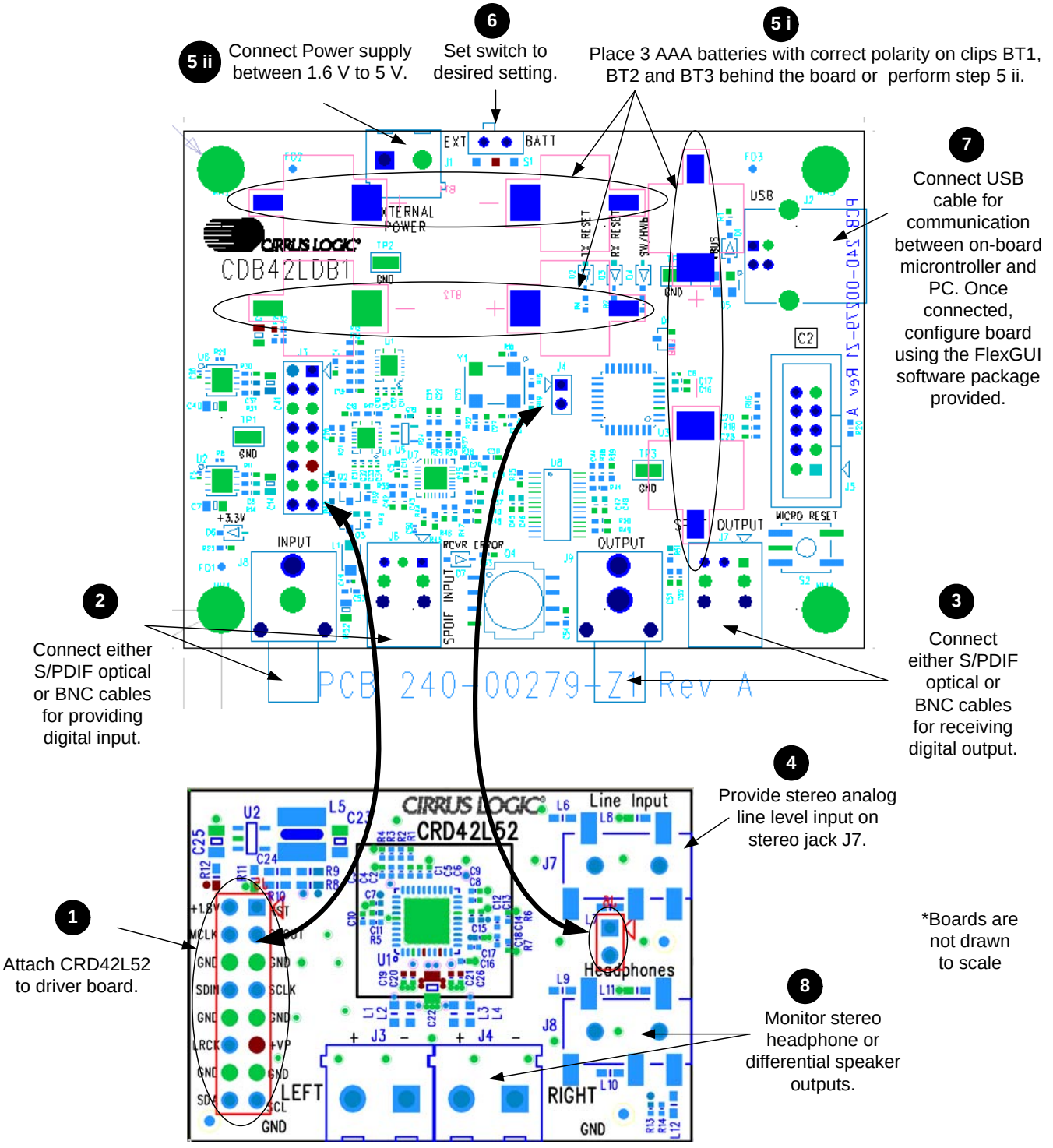


Figure 1. Quick-Start Guide

3. CONFIGURATION OPTIONS

This section provides a deeper understanding of on-board circuitry and digital clock and data signal routing for appropriately setting the control software in a specific configuration. The section also provides the expected performance characteristics for the respective configuration mode.

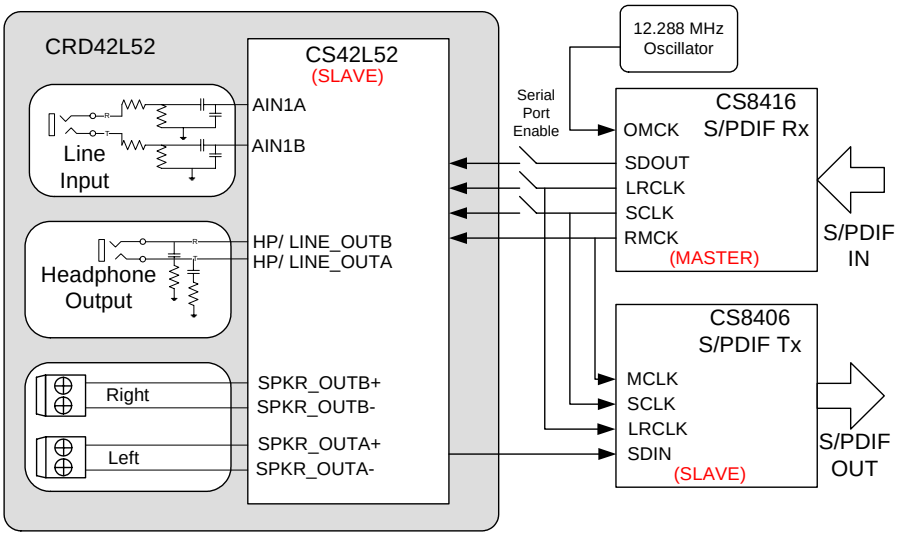


Figure 2. CRD42L52 and CDB42LDB1 Block Diagram for ADC and DAC Testing

In order to test the ADC, DAC and PWM on the CS42L52, S/PDIF digital input needs to be provided to the CS8416 S/PDIF receiver on the CDB42LDB1 driver board via optical or RCA input jacks. The CS8416 operates in master mode and drives the serial audio interface lines to the CS42L52 and the CS8406, as shown in Figure 2. For correct CS42L52 serial port operation, the CS42L52 serial port should be set up as a slave and the “Driver Board Serial Port” needs to be enabled in the FlexGUI software.

3.1 S/PDIF In to Headphone Out

Stereo headphone-level analog outputs can be monitored on stereo jack J8 on the CRD42L52. Serial Audio digital clocks and data is routed to the CRD42L52 via I/O header J3. Table 1 shows expected performance characteristics when the boards are configured to make digital input to analog output measurements.

Plot	Location
FFT - S/PDIF In to Headphone Out @ 0 dBFS	Figure 12 on page 15
FFT - S/PDIF In to Headphone Out @ -60 dB FS	Figure 13 on page 16
Dynamic Range - S/PDIF In to Headphone Out	Figure 14 on page 16
Frequency Response - S/PDIF In to Headphone Out	Figure 15 on page 16
THD + N - S/PDIF In to Headphone Out	Figure 16 on page 16

Table 1. S/PDIF In to Headphone Out Performance Plots

3.2 Line In to S/PDIF Out

Line-level analog input can be provided to the CS42L52 via stereo jack J7 on the CRD42L52. The analog input path on the CRD42L52 scales the input down to a fifth of its actual value. Therefore, a 2.4 Vrms analog input into the CRD42L52 is required to provide full-scale input to the CS42L52. The ADC core uses the clocks provided to the CS42L52 by the CS8416 to perform the conversion and outputs data to the CS8406 S/PDIF transmitter on the CDB42LDB1 driver board via the I/O header, J3. The S/PDIF output can be monitored on the RCA or optical jacks (J9 and J7).

Table 2 shows expected performance characteristics when the boards are configured to make analog input to digital output measurements.

Plot	Location
Dynamic Range - Line In to S/PDIF Out	Figure 9 on page 15
Frequency Response - Line In to S/PDIF Out	Figure 10 on page 15
THD + N - Line In to S/PDIF Out	Figure 11 on page 15

Table 2. Line In to S/PDIF Out Performance Plots

3.3 S/PDIF In to Speaker Out

Stereo differential speaker outputs from the CS42L52 can be monitored on screw terminals J3 and J4. The CS42L52 can be set up to provide data to the PWM modulator for producing speaker outputs from either the serial port PCM input or the ADC output using the FlexGUI software. For a description of the Cirrus FlexGUI software controls, refer to Section 4 on page 9. Table 3 shows expected performance characteristics when the boards are configured to make speaker output measurements.

Plot	Location
Frequency Response - S/PDIF In to Speaker Out	Figure 17 on page 16

Table 3. S/PDIF In to Speaker Out Performance Plots

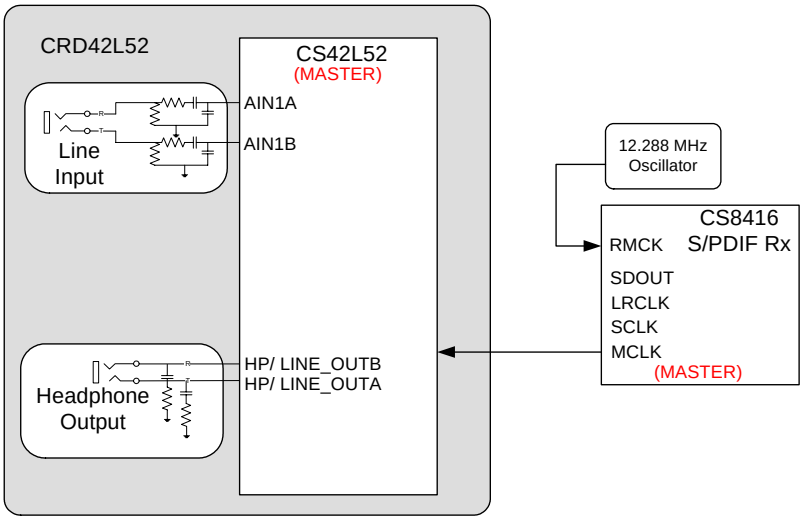


Figure 3. CRD42L52 and CDB42LDB1 Block Diagram for Digital Loopback Testing

3.4 Analog In to Analog Out - Digital Loopback

In order to use the CS42L52 in digital loopback mode, one can configure the CS42L52 to operate in master or slave mode. Figure 3 shows the board configuration when the CODEC is set up to operate in master mode. In this mode, the CS42L52 receives an MCLK from the driver board from the CS8416 S/PDIF reciever. As described in Section 1.3 on page 4 and shown in Figure 3, the S/PDIF receiver uses the on-board 12.288 MHz clock as an MCLK when it is not receiving a S/PDIF input stream. Table 3 shows expected performance characteristics when the boards are configured to make speaker output measurements.

Plot	Location
Dynamic Range - Line In to HP Out (Digital Loopback)	Figure 18 on page 16
THD + N - Line In to HP Out (Digital Loopback)	Figure 19 on page 17

4. SOFTWARE MODE CONTROL

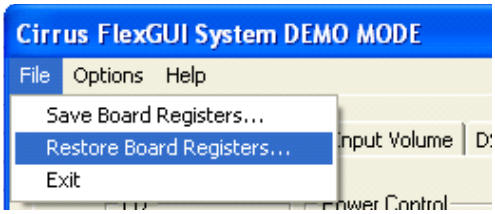
The CRD42L52 may be used with the CDB42LDB1 driver board and the Microsoft® Windows-based FlexGUI graphical user interface, allowing software control of the CS42L52 and FPGA registers. The latest control software may be downloaded from **www.cirrus.com/msasoftware**. Step-by-step instructions for setting up the FlexGUI are provided as follows:

1. Download and install the FlexGUI software as instructed on the Website.
2. Apply power using either an external source connected to screw terminal J1 or 3 AAA batteries (not included) on BT1, BT2 and BT3.
3. Connect the CDB42LDB1 to the host PC using a USB cable.
4. Launch the Cirrus FlexGUI. *Once the GUI is launched successfully, all registers are set to their default reset state.*
5. Refresh the GUI by clicking on the **Update** button. *The default state of all registers are now visible.*

For standard set-up:

6. Set up the CS42L52 in the CODEC Configuration, Analog Input Volume Control, DSP Engine or Analog and PWM Output Volume Controls tab as desired.
7. Begin evaluating the CS42L52.

For quick set-up, the CRD42L52 may, alternatively, be configured by loading a predefined sample script file:



8. On the File menu, click **Restore Board Registers...**
9. Browse to Boards\CRD42L52\Scripts\.
10. Choose any one of the provided scripts to begin evaluation.

To create personal script files:

11. On the File menu, click **Save Board Registers...**
12. Enter any name that sufficiently describes the created setup.
13. Choose the desired location and save the script.
14. To load this script, follow the instructions from step 8 above.

4.1 CODEC Configuration Tab

The “CODEC Configuration” tab provides high-level control of various configurations for the CRD42L52. Status text detailing the CODEC’s specific configuration appears directly below the associated control. This text will change depending on the setting of the associated control. A description of each group is outlined below. See the CS42L52 data sheet for complete register descriptions.

Power Control - Includes register controls for powering down the CODEC, ADC, PGA, headphone and speaker amplifiers. Microphone power register controls are not included as they are not connected on the CRD42L52 and are powered down by default.

ADC Input Configuration - Includes controls for the internal PGA MUX and analog inputs.

Serial Port Configuration - Includes controls for all settings related to the transmission and relationship of data and clocks within the CODEC.

Driver Board Serial Port Disable - Controls the switch that allows the CDB42LDB1 to drive the data/clock I/O lines going to the CDB42LDB1 reference design board.

Update - Reads all registers in the CS42L52 and reflects the current values in the GUI.

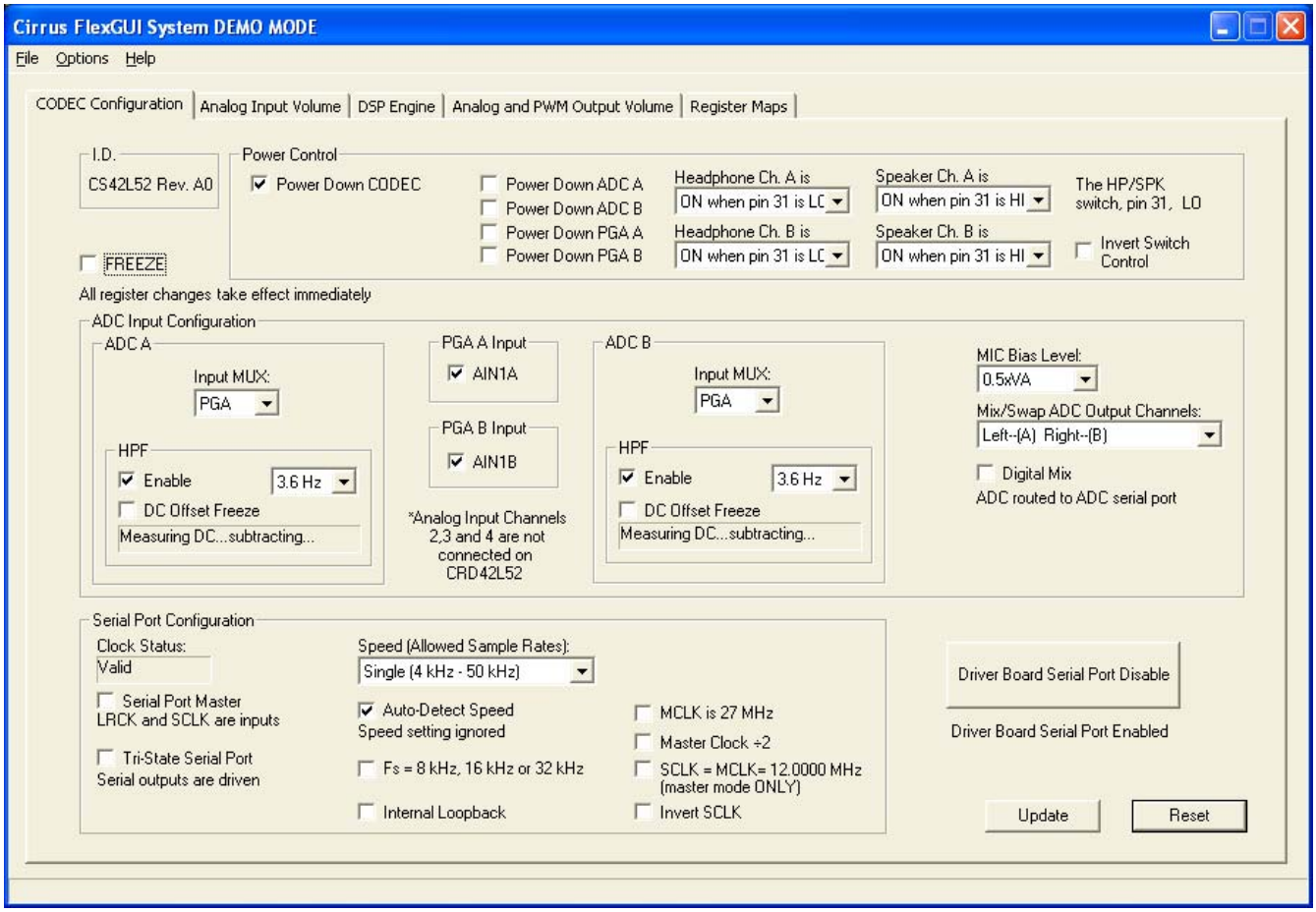


Figure 4. CODEC Configuration Tab

4.2 Analog Input Volume Tab

The “Analog Input Volume” tab provides high-level control of all volume settings in the ADC of the CS42L52. Status text detailing the CODEC’s specific configuration is shown inside the control group of the affected control. This text will change depending on the setting of the associated control. A description of each group is outlined below. See the CS42L52 data sheet for complete register descriptions.

Digital Volume Control - Includes digital volume controls and adjustments for the ADC.

ALC Configuration - Includes all configuration settings for the Automatic Level Control (ALC).

Analog Volume Control - Includes all analog volume controls and adjustments for the PGA.

Noise Gate Configuration - Includes all configuration settings for the noise gate.

Update - Reads all registers in the CS42L52 and reflects the current values in the GUI.

Reset - Resets the CS42L52.

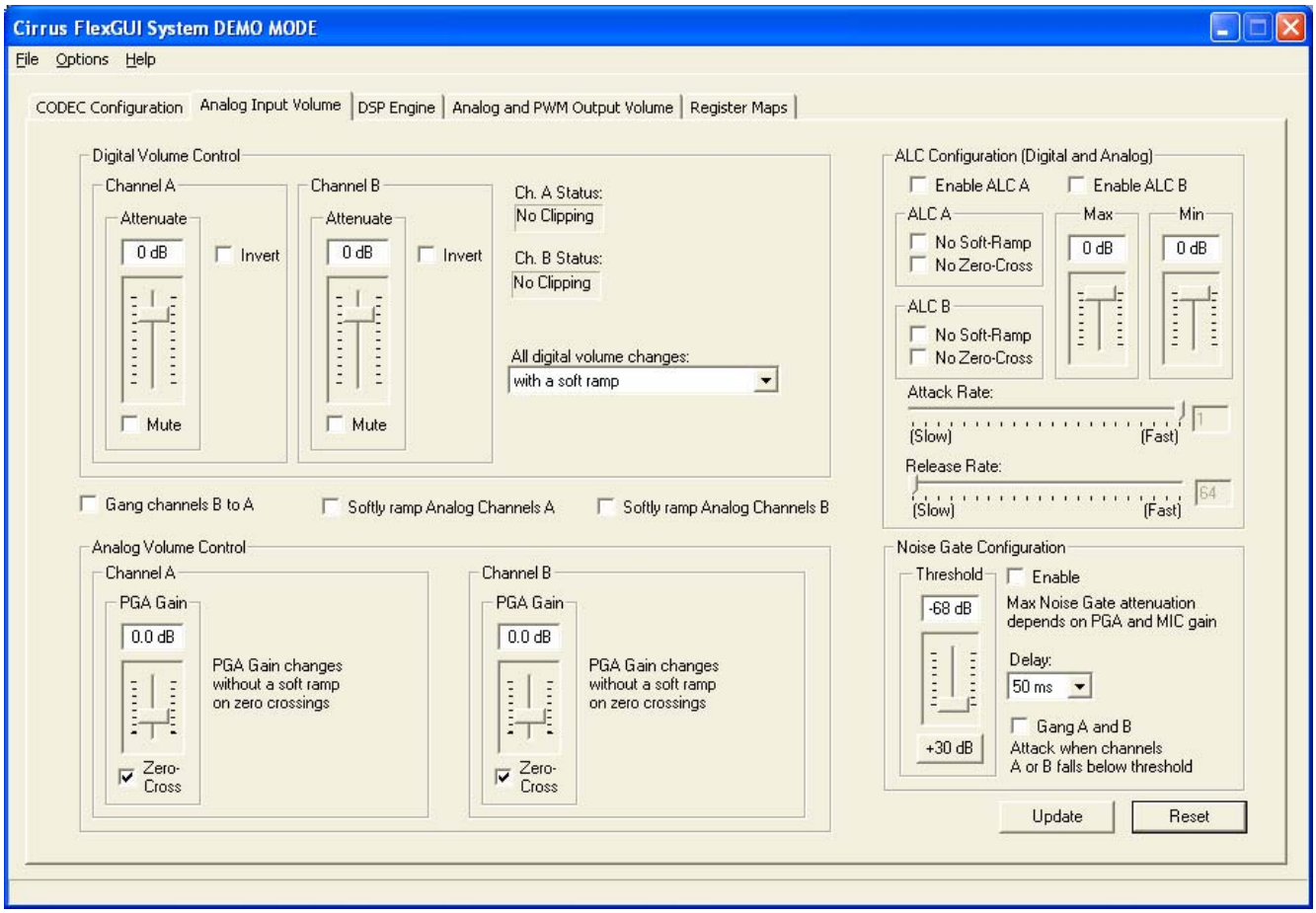


Figure 5. Analog Input Volume Tab

4.3 DSP Engine Tab

The “DSP Engine” tab provides high-level control of the SDIN (PCM) data volume level, the ADC output/SDIN mix volume level and the overall DAC/PWM channel volume level. DAC/PWM channel Limiter, Tone Control and Beep Generator control functions are also provided.

Status text detailing the CODEC’s specific configuration is shown inside the control group of the affected control. This text will change depending on the setting of the associated control. A description of each group is outlined below. See the CS42L52 data sheet for complete register descriptions.

Digital Volume Control - Digital volume controls and adjustments for the SDIN data, ADC out data and overall channel volume. Mute, gang, invert and de-emphasis functions are also available.

Limiter - Configuration settings for the Automatic Level Control (ALC).

Tone Control - Bass and treble volume controls and filter corner frequencies.

Beep Generator - On/Off time, frequency, volume, mix and repeat beep functions.

Update - Reads all registers in the CS42L52 and reflects the current values in the GUI.

Reset - Resets the CS42L52.

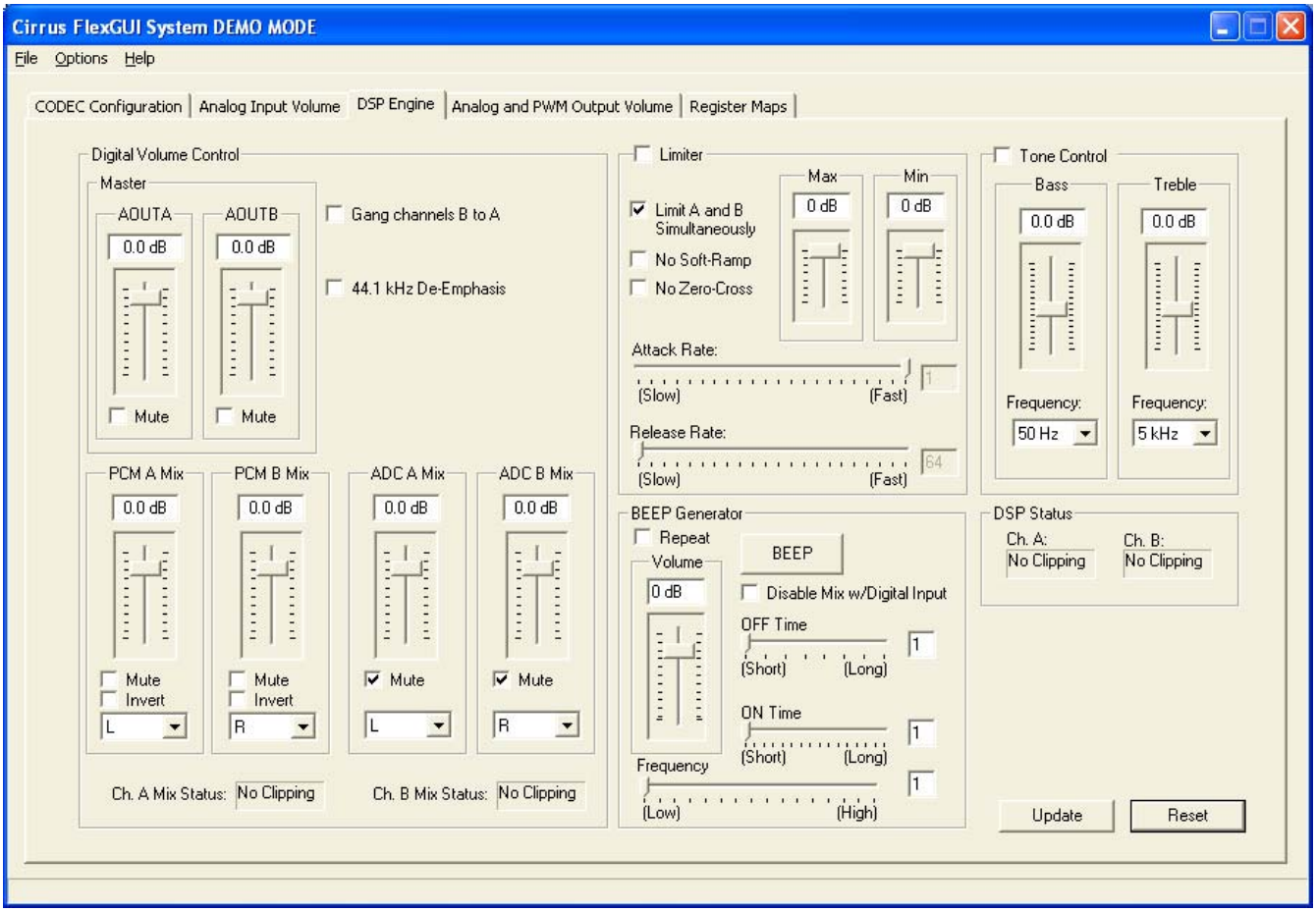


Figure 6. DSP Engine Tab

4.4 Analog and PWM Output Volume Tab

The “Analog and PWM Output Volume” tab provides high-level control of the CS42L52 input passthrough volume, HP/Line output volume levels, charge pump frequency, speaker volume, and PWM Temperature/Battery monitoring controls. Status text detailing the CODEC’s specific configuration appears directly below the associated control. This text will change depending on the setting of the associated control. A description of each group is outlined below. See the CS42L52 data sheet for complete register descriptions.

Headphone/Line Analog Output - Digital volume controls and adjustments for the DAC channel (outside of the DSP) and for the input passthrough. The modulation index and gain settings make up the parameters that determine the full scale headphone/line output level.

PWM Output - Volume, mute, power down and other functional controls for the PWM speaker outputs.

Temperature and Battery Monitor/Control - Battery Compensation, Thermal Foldback, Temperature Shutdown and Battery Monitor for the PWM/Speaker outputs.

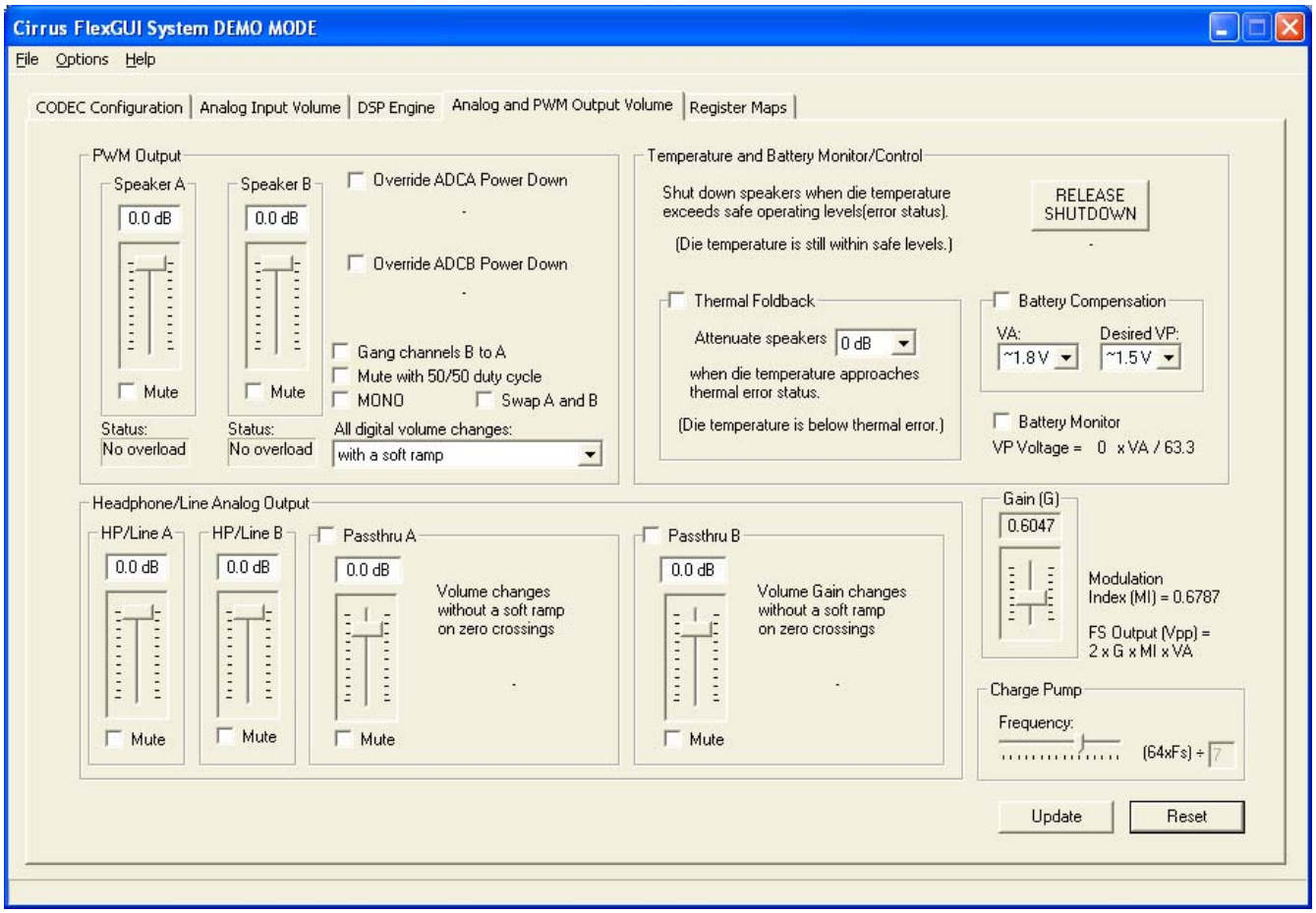
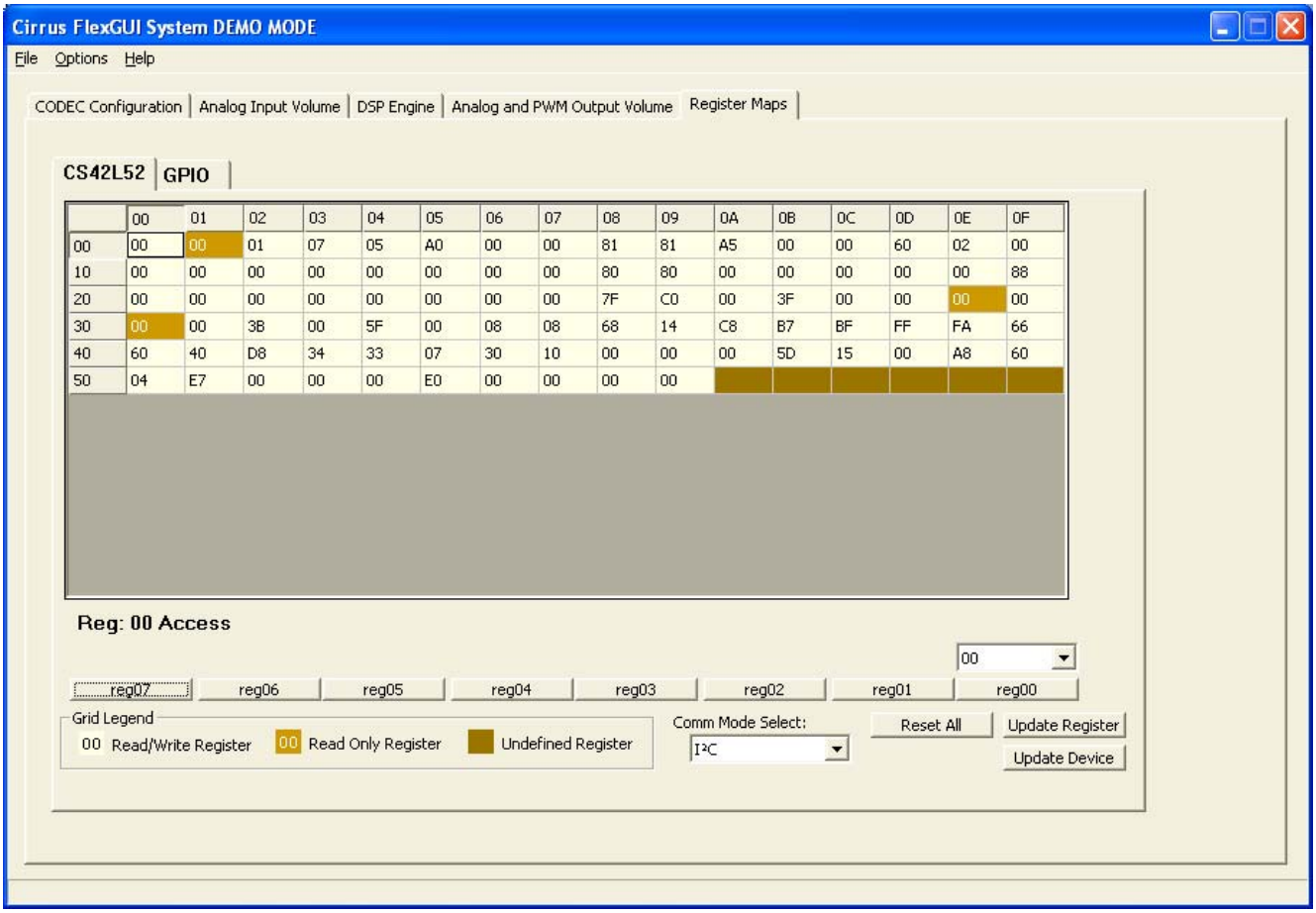


Figure 7. Analog and PWM Output Volume Tab

4.5 Register Maps Tab

The Advanced Register Debug tab provides low-level control of the CS42L52 individual register settings. Register values can be modified bit-wise or byte-wise. For bit-wise, click the appropriate push-button for the desired bit. For byte-wise, the desired hex value can be typed directly into the register address box in the register map. The “GPIO” tab may be ignored.



	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
00	00	00	01	07	05	A0	00	00	81	81	A5	00	00	60	02	00
10	00	00	00	00	00	00	00	00	80	80	00	00	00	00	00	88
20	00	00	00	00	00	00	00	00	7F	C0	00	3F	00	00	00	00
30	00	00	3B	00	5F	00	08	08	68	14	C8	B7	BF	FF	FA	66
40	60	40	D8	34	33	07	30	10	00	00	00	5D	15	00	A8	60
50	04	E7	00	00	00	E0	00	00	00	00						

Figure 8. Register Maps Tab

5. PERFORMANCE PLOTS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 20 Hz to 20 kHz (unweighted); VA=VD=VA_HP=1.8 V; Sample Frequency = 48 kHz; HP test load: R_L = 10 kΩ.

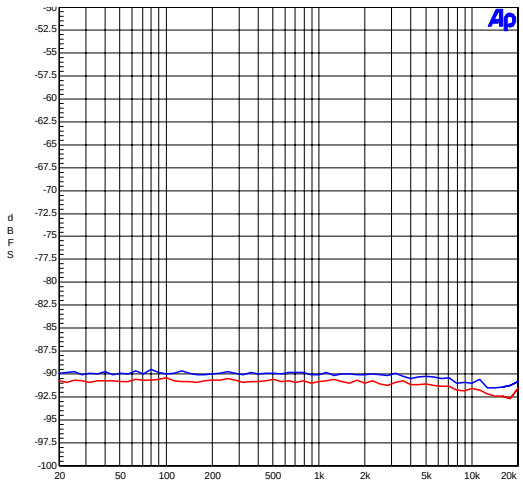


Figure 9. Dynamic Range - Line In to S/PDIF Out

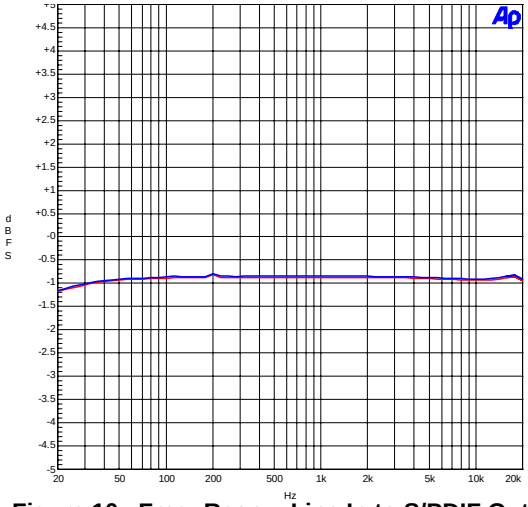


Figure 10. Freq. Resp. - Line In to S/PDIF Out

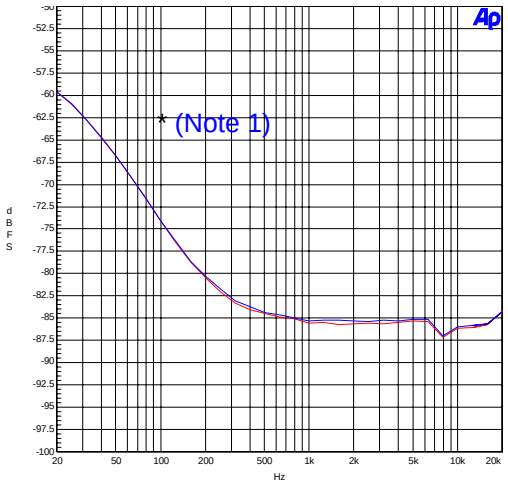


Figure 11. THD + N - Line In to S/PDIF Out

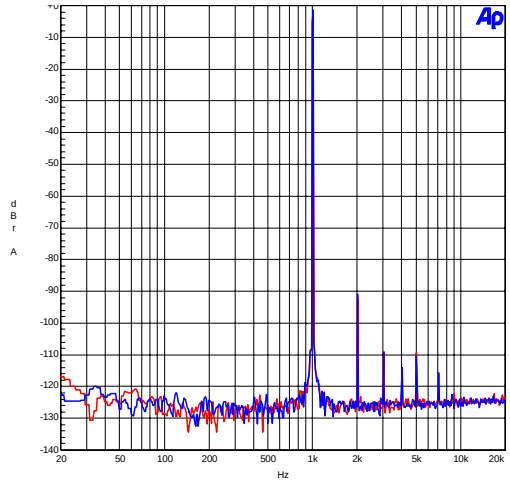


Figure 12. FFT - S/PDIF In to HP Out @ 0 dBFS

Notes:

1. The total harmonic distortion + noise (THD+N) performance of the ADC in the CS42L52 is determined by the value of the capacitor on the FILT+ pin. Larger capacitor values yield significant improvement in THD+N at low frequencies. A 1 uF capacitor was used to make the performance measurement in Figure 12.

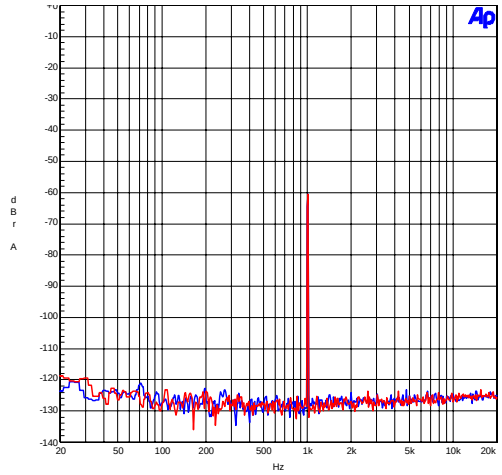


Figure 13. FFT - S/PDIF In to HP Out @ -60 dBFS

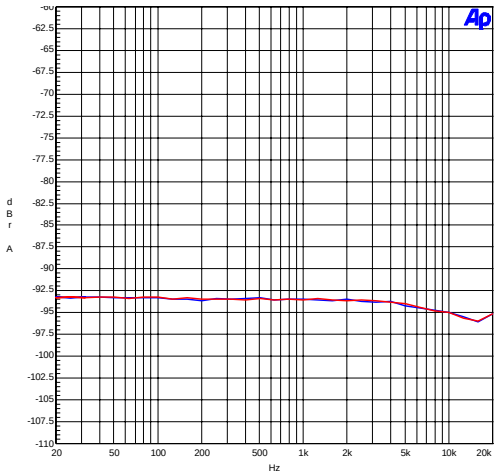


Figure 14. Dynamic Range - S/PDIF In to HP Out

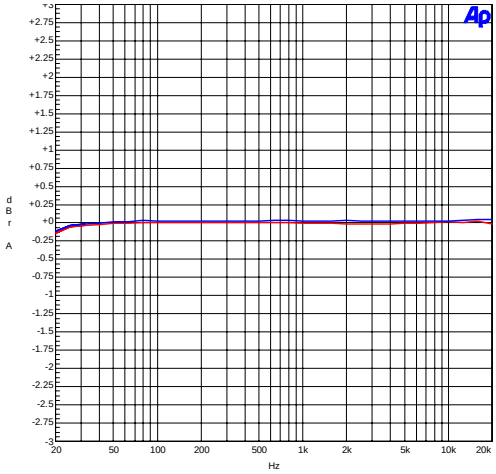


Figure 15. Freq. Resp. - S/PDIF In to HP Out

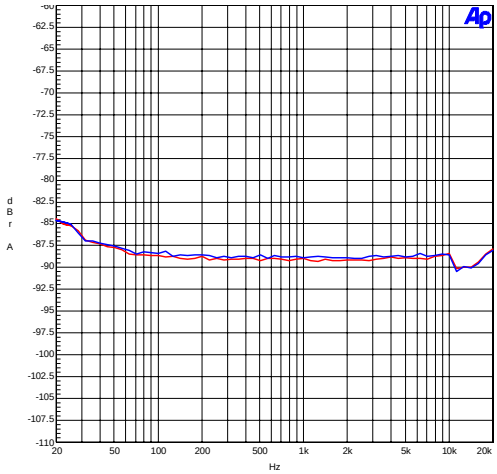


Figure 16. THD + N - S/PDIF In to HP Out

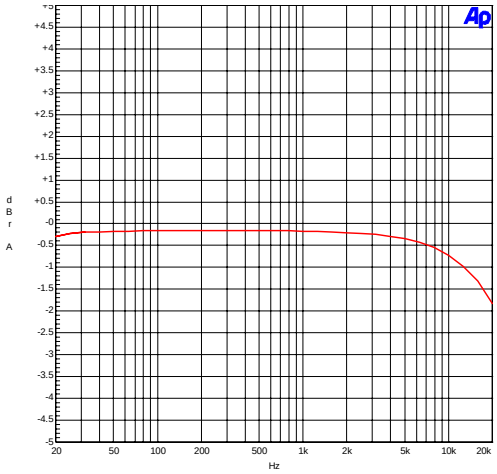


Figure 17. Freq. Resp. - S/PDIF In to Spkr. Out

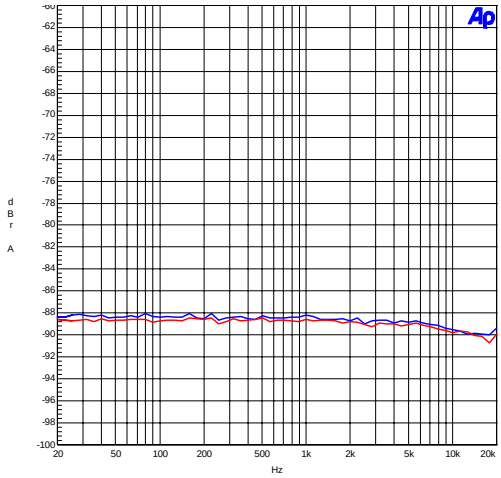


Figure 18. Dynamic Range - Line In to HP Out (Dig. LB)

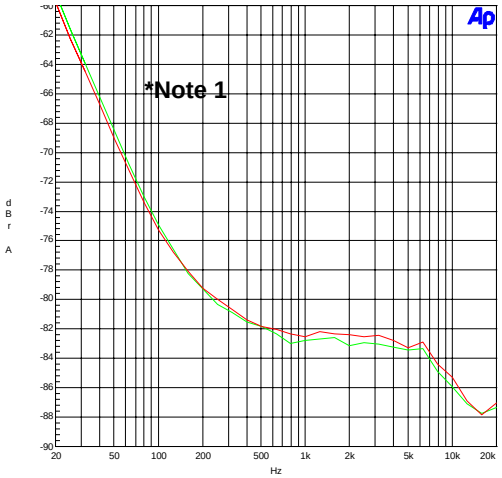


Figure 19. THD + N - Line In to HP Out (Dig. LB)

6. SYSTEM CONNECTIONS & INTERFACE

On CDB42LDB1:

Connector/ Interface	Reference Designator	Input/ Output	Description
AAA	BT1 BT2 BT3	Input	Battery Power Supply.
Power Supply Switch	S1	Input	Switch that selects which power supply is used by the CDB42LDB1 and the CRD42L52.
External Power	J1	Input	+5 V - +2.7 V external power supply.
USB	J2	Input/Output	USB connection to PC for I²C control port signals.
S/PDIF OPTICAL OUT	J7	Output	CS8406 digital audio output via optical cable.
S/PDIF COAX OUT	J9	Output	CS8406 digital audio output via coaxial cable.
S/PDIF OPTICAL IN	J6	Input	CS8416 digital audio input via optical cable.
S/PDIF COAX IN	J8	Input	CS8416 digital audio input via coaxial cable.
MICRO JTAG	J5	Input/Output	I/O for programming the micro controller (U3).
MICRO RESET	S4	Input	Reset for the micro controller (U3).
I/O Header	J3	Input/Output	I/O routing between CDB42LDB1 and CRD42L52 containing Control Port and Serial Audio Clock and Data .

On CRD42L52:

Connector/ Interface	Reference Designator	Input/ Output	Description
Line Input	J7	Input	Stereo jack for line level input signal to analog input channel 1 on CS42L52.
Headphones	J8	Output	Stereo jack for monitoring stereo headphone output from CS42L52.
SPEAKER LEFT SPEAKER RIGHT	J3 J4	Output	Screw Terminals for monitoring differential stereo speaker output from CS42L52.
I/O Header	J5	Input/Output	I/O routing between CDB42LDB1 and CRD42L52 containing Control Port and Serial Audio Clock and Data .

CRD42L52 AND CDB42LDB1 BLOCK DIAGRAM

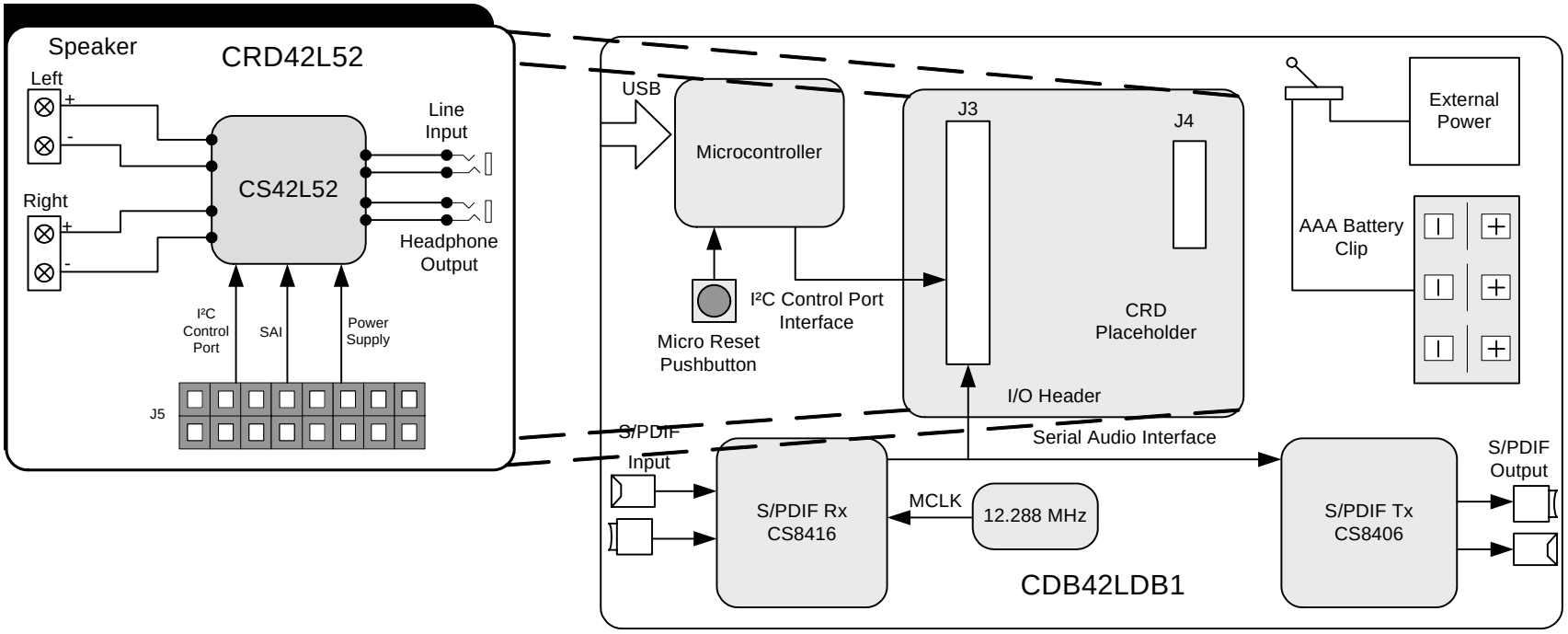


Figure 20. Block Diagram

7. CRD42L52 SCHEMATICS

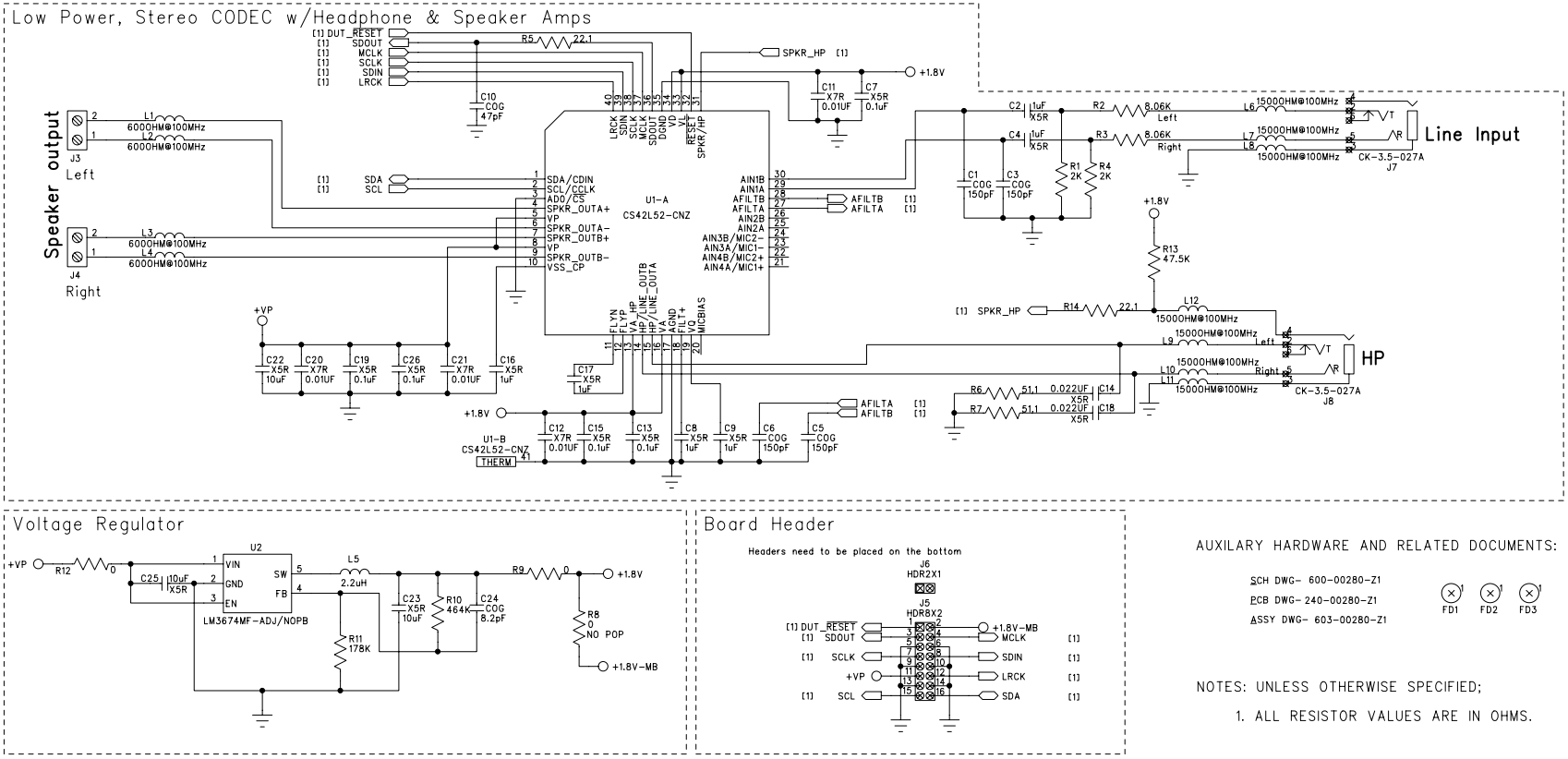


Figure 21. CS42L52 and Analog I/O

8. CDB42LDB1 SCHEMATICS

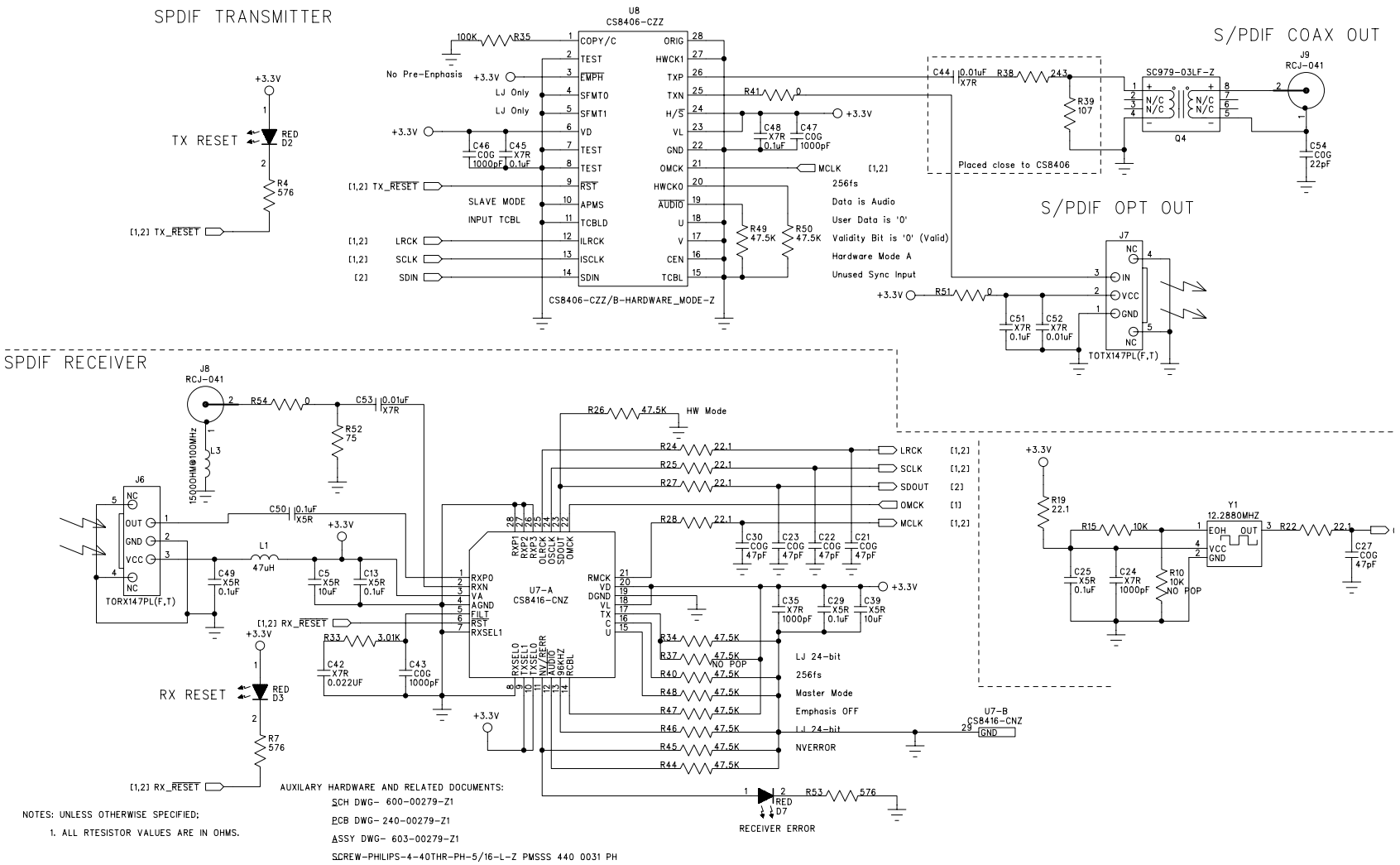


Figure 22. S/PDIF Input/Output

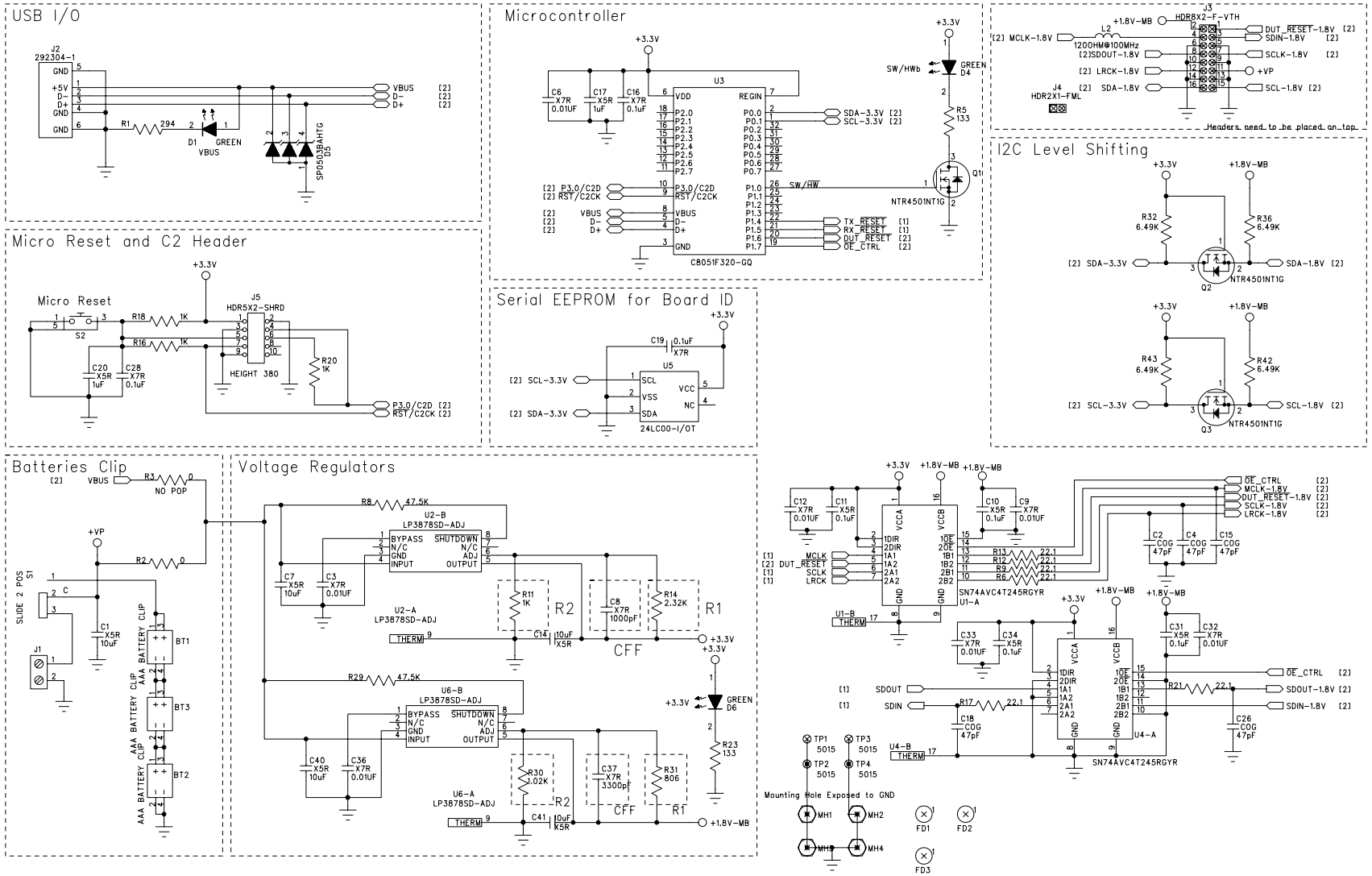


Figure 23. Microcontroller, Push Buttons and LED Indicators

9. CRD42L52 LAYOUT

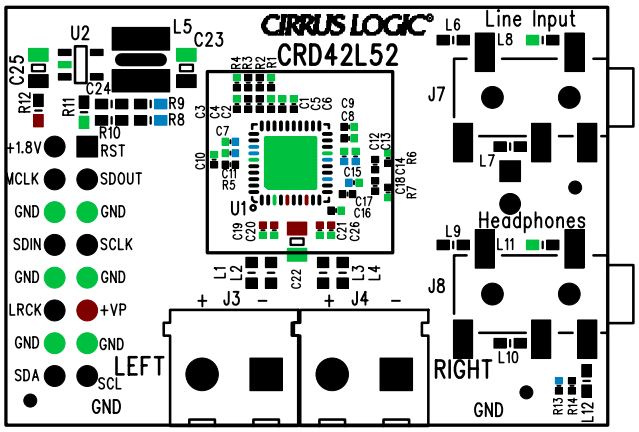


Figure 24. Silkscreen Top

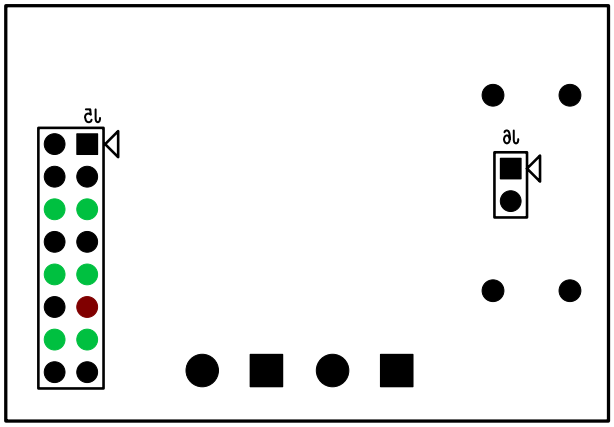


Figure 25. Silkscreen Bottom

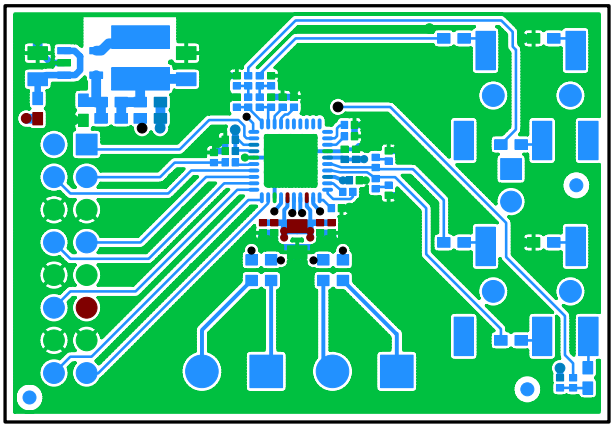


Figure 26. Top-Side Layer

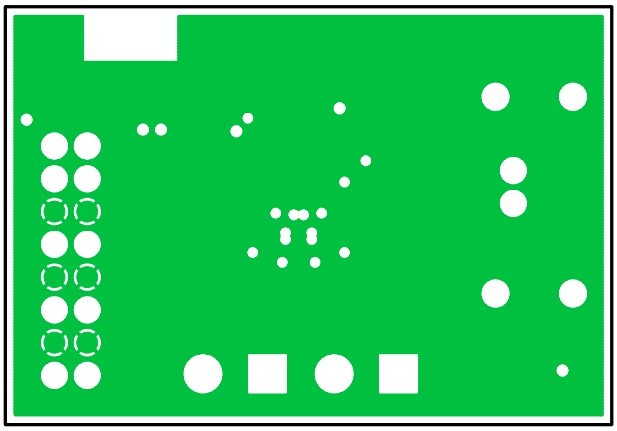


Figure 27. Internal Layer (Ground Plane)

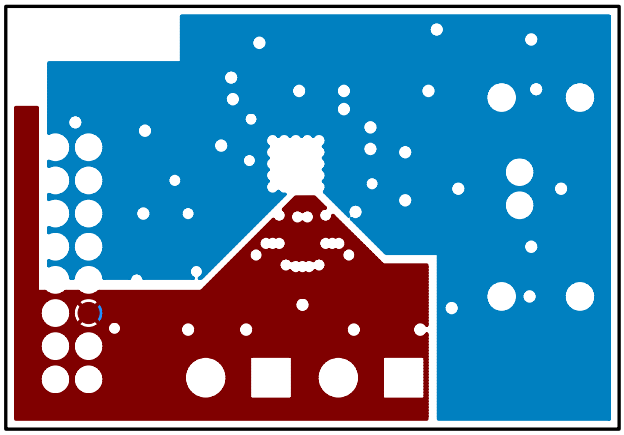


Figure 28. Internal Layer (Power Plane)

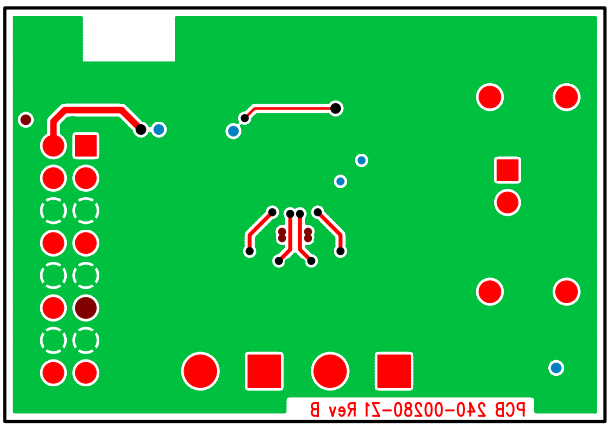


Figure 29. Bottom-Side Layer

10.CDB42LDB1 LAYOUT

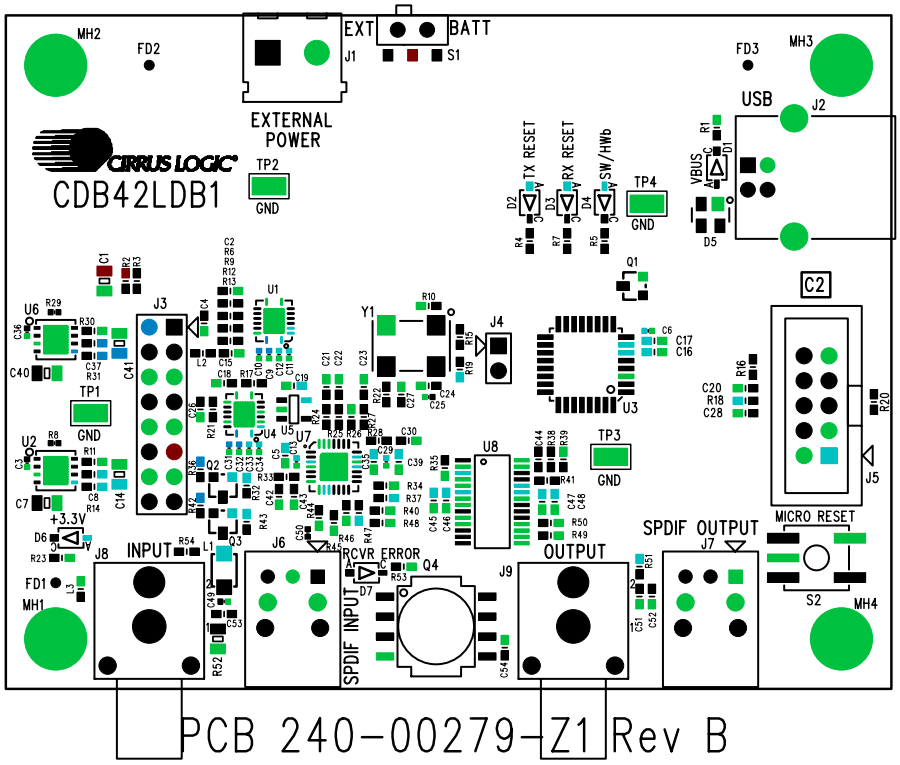


Figure 30. Silkscreen Top

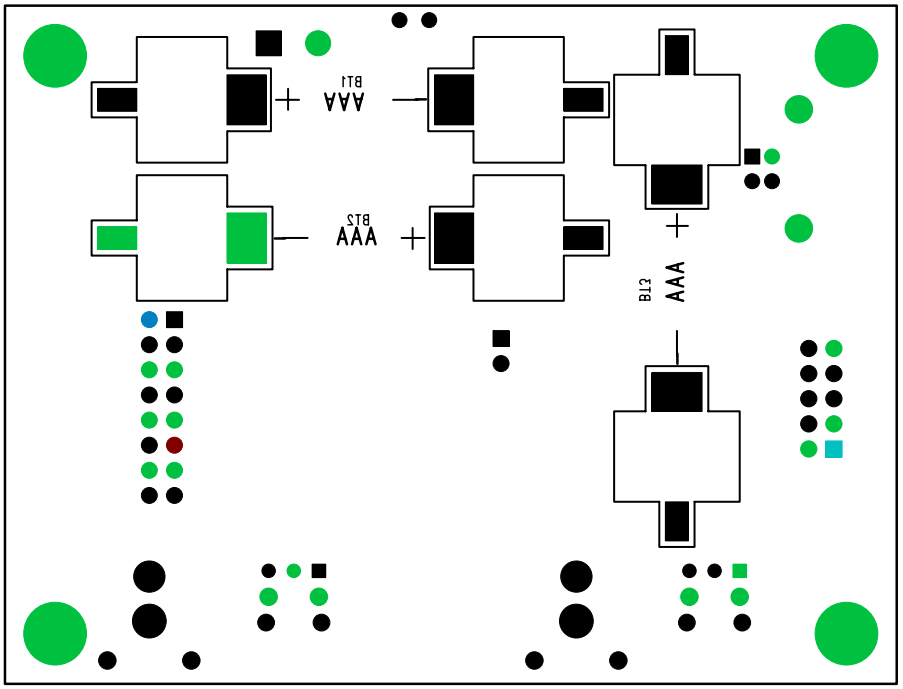


Figure 31. Silkscreen Bottom

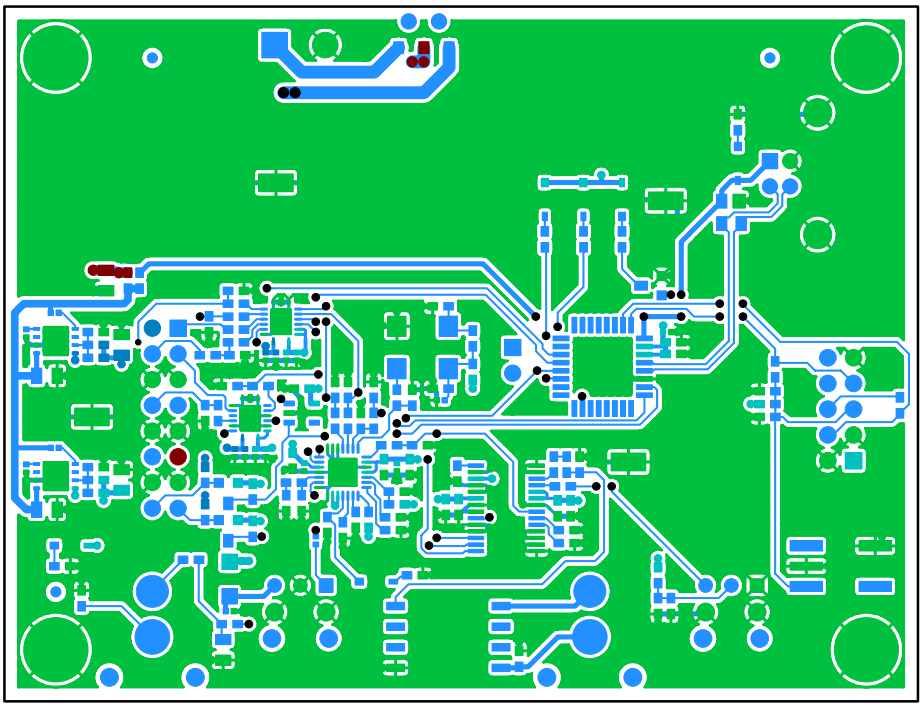


Figure 32. Top-Side Layer

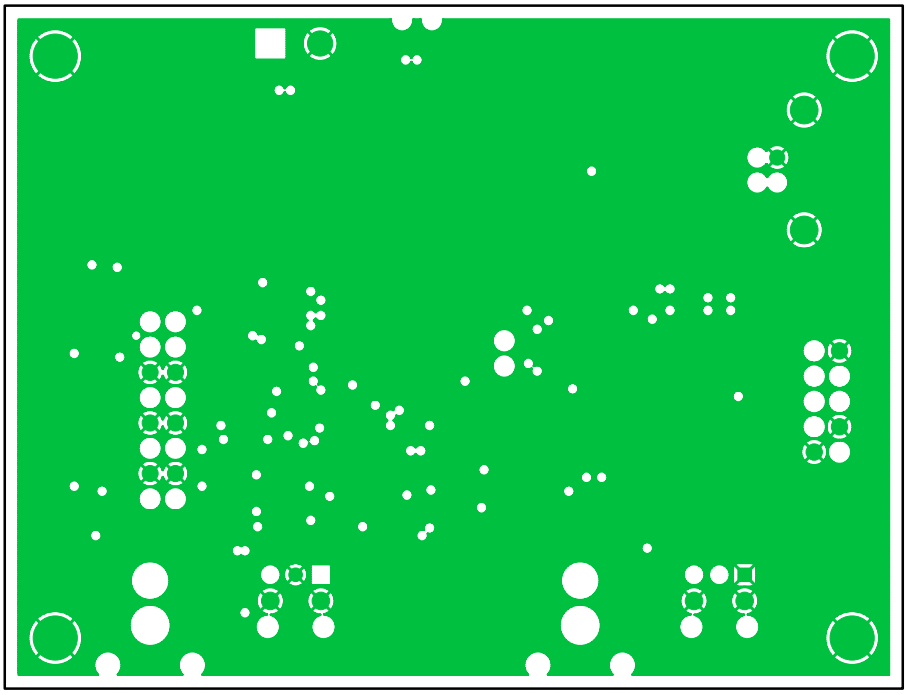


Figure 33. Layer 2

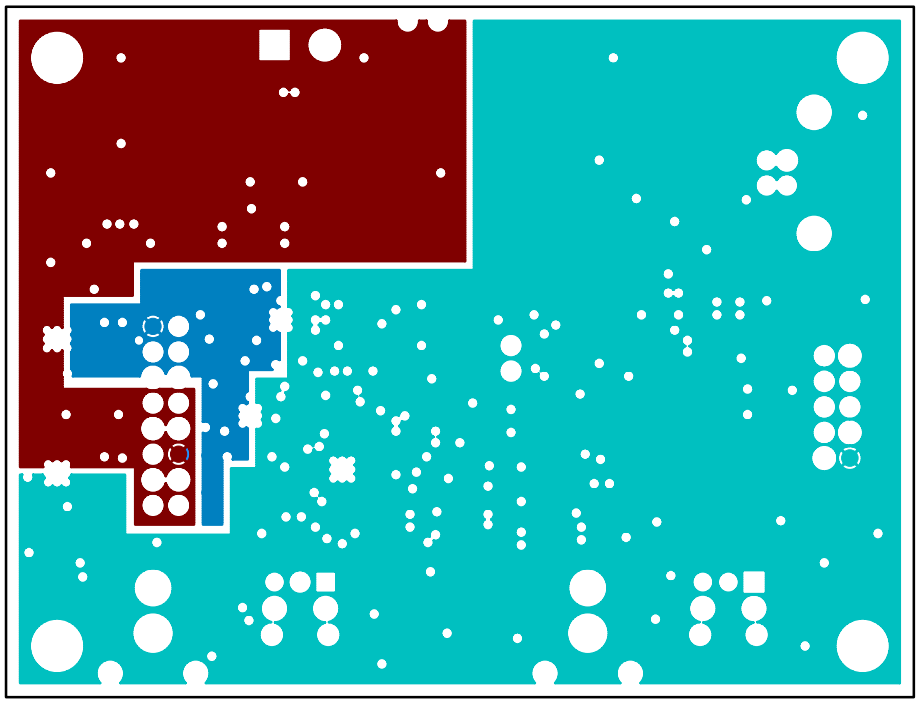


Figure 34. Layer 3

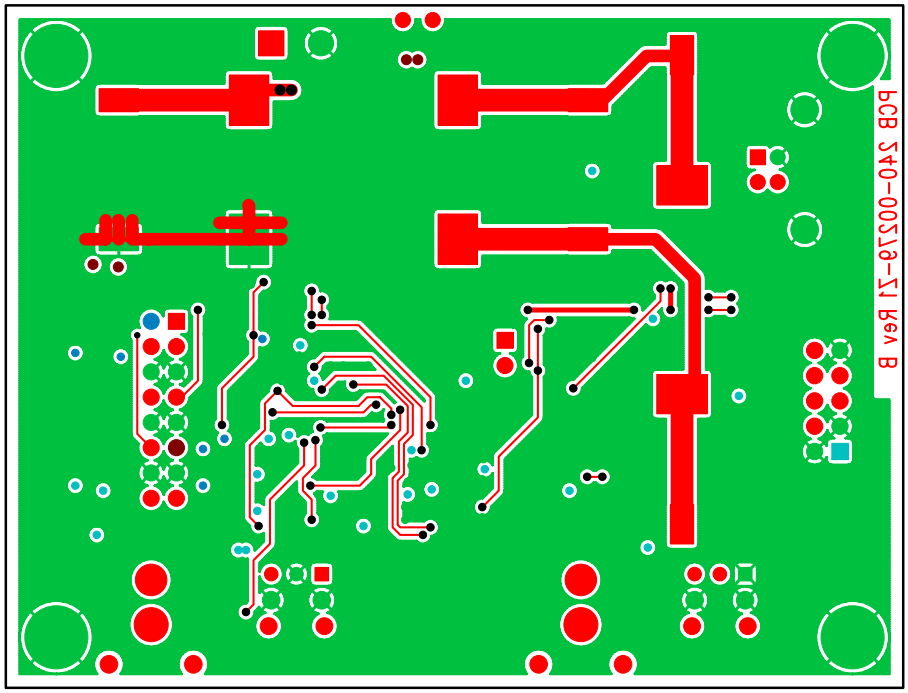


Figure 35. Bottom-Side Layer

11.REVISION HISTORY

Release	Changes
RD1	Initial Release

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.